Amendments to the Specification

Please replace the paragraph at page 3, lines 18 through 20 with the following amended paragraph:

The portion of the non-binary width data structure stored per logical row in the first binary memory block stores twelve entries, the first other portion stored per logical row in the second binary memory block stores four entries and the second other portion stored per logical row in the second binary memory stores four entries. The width of the entry is 21-bits, the non-binary data structure stores 16 entries and n is 15. Twelve of the sixteen entries in the non-binary width data structure are stored in the first binary memory block and the other four entries are stored in the first other portion or the second other portion of the second binary memory block.

Please replace the paragraph at page 6, lines 1 through 11 with the following amended paragraph:

Continuing with Fig. 1C, the subtree entry 404 provides access to 256 possible routes one for ~~to~~ each node on the bottom level of subtree A. The routes are stored in mapper entries 420 in the subtree mapper 418. To provide access to 256 possible routes, a dense subtree descriptor is stored in the data field 406. A dense subtree descriptor includes a bit for each node at the bottom level of the subtree. Thus, for an 8-level subtree, the data field 406 is 256 bits wide, providing one bit for each node at the bottom level of the subtree. A bit in the data field 406 is set to '0' if the route for the previous node is to be used and set to '1' to use the next route stored in the subtree mapper 418. The subtree mapper 418 has 2^{19} (512K) locations for storing mapper entries 420, with 2^4 (16) mapper entries 420 stored in each of the 2^{15} (32K) logical rows. The mapper address 416 is nineteen bits to index the 2^{19} (512K) mapper entries 420.

Please replace the paragraph at page 6, lines 12 through 20 with the following amended paragraph:

A mapper entry 420 is 21-bits wide. The pointers field 408 is 256 bits wide to allow for the storage of sixteen 16-bit pointers. Each pointer stores a 15-bit base address for a block of 16 contiguous mapper entries 420 in the subtree mapper 418. Thus, the pointers field 408 can indirectly provide a pointer to a mapper entry 420 in the subtree mapper 418 for each node in the bottom level of subtree A. The data field 406, pointers field 408 and mapper entry 420 are described in ~~co-pending~~ U.S. Patent Application Serial No. 09/733,627 entitled "Method and Apparatus for Longest Match Address Lookup," filed December 8, 2000 by David A. Brown which issued as U.S. Patent No. 6,691,218 on February 10, 2004 incorporated herein by reference in its entirety.

Please replace the paragraph at page 8, lines 12 through 17 with the following amended paragraph:

Mapper logic 304 maps logical memory addresses LA18- LA0 to physical memory addresses to provide the logical expanded non-binary width view shown in Fig. 2B of ~~a~~ physical binary macro cells 204, 206 shown in Fig. 2A. The data structure including 16 non-binary entries is logically stored in a single logical memory row but is physically stored in a first physical macro cell 204 and a second physical macro cell 206.

Please replace the paragraph at page 12, lines 20 through 23 with the following amended paragraph:

Fig. 4 ~~is~~ illustrates the subtree memory including a single memory macro cell for storing a non-binary data structure according to the principles of the present invention. In the alternative embodiment shown in Fig. 4, the logical memory shown in Fig. 2B can be implemented as a single macro cell 400.